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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: KOJI SUZUKI

For: METHOD OF MANUFACTURING THIN FILM TRANSISTOR

LETTER

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Dear Sir:

The attached application for U.S. Patent is being filed under the provisions of Rule 1.53 of the Rules of Practice in Patent and Trademark cases. Accordingly, we are enclosing the following documents at this time:

- (a) Specification and abstract (20 pages) and Claims (12 claims); and
- (b) Drawings (4 sheets)

The filing fee, Declaration and Assignment documents will be submitted later under the provisions of 37 CFR 1.53.

Please be advised that the inventor of the invention disclosed in the attached specification and claims is: KOJI SUZUKI, residing at 1, Tsujimae, Mitsuouji, Kisogawa-cho, Haguri-gun, Aichi, Japan.

Please also be advised that the undersigned has been authorized to file this application on his behalf.



If there are any additional charges with respect to this patent application or otherwise, please charge them to Deposit Account No. 06-1130 maintained by Applicant's attorney.

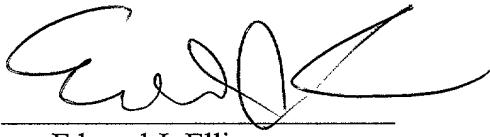
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Respectfully submitted,

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**METHOD OF MANUFACTURING THIN FILM TRANSISTOR**

**BACKGROUND OF THE INVENTION**

5    1. Field of the Invention

The present invention relates to a method of manufacturing a thin film transistor.

2. Description of Related Art

10       Thin film transistors (hereinafter referred to as a "TFT" or "TFTs") employing, as an active layer, a p-Si film formed on a transparent insulating substrate are being developed as pixel drive elements in active matrix type LCDs (Liquid Crystal Displays).

15       Poly-silicon thin film transistors (hereinafter referred to as "p-Si TFTs") are more advantageous than amorphous silicon thin film transistors (hereinafter referred to as "a-Si TFTs") because they have a larger mobility and a higher driving ability. Therefore, the p-Si TFTs allow implementation of LCDs 20 with high performance, in which, along with pixel portions, peripheral driving circuits can also be integrated on the same substrate.

25       In a p-Si TFT, so as to form source and drain regions in the p-Si film functioning as an active layer, the p-Si film is subjected to ion doping followed by a thermal processing for activation.

A method of manufacturing a TFT according to a related art will be described. Fig. 1 is a cross section of a TFT fabricated by a TFT manufacturing method according to a related art.

5 Referring to Fig. 1, a first gate insulating film 13 comprising an SiO<sub>2</sub> film and a second gate insulating film 14 comprising an SiN film disposed thereon are formed over the entire surface of a substrate 10 so as to include a p-Si film 12.

10 In Figs. 2A to 2D, cross sections of a TFT are depicted to illustrate the TFT manufacturing process steps according to the related art.

Step 1 (Fig. 2A):

15 On an insulating substrate 10 comprising a quartz glass, non-alkali glass or the like, an SiO<sub>2</sub> film 11 serving as an insulating protective film is formed by the plasma CVD method, and an a-Si film 12 is formed on the SiO<sub>2</sub> film 11 using plasma CVD method. Then, the a-Si film 12 is subjected to annealing by scanning to irradiate the surface thereof with an excimer 20 laser such that the a-Si film 12 is molten and recrystallized to a p-Si film 12, which is then etched into an island shape functioning as an active layer.

Step 2 (Fig. 2B):

25 The first gate insulating film 13 comprising an SiO<sub>2</sub> film and the second gate insulating film 14 comprising an SiN film are stacked over the entire surface of the p-Si film 12 by the

CVD method. A conductive material comprising a refractory metal such as chromium (Cr) or molybdenum (Mo) is then deposited on the SiN film 14 using a sputtering method so as to form a gate electrode 15 such that it superposes the 5 semiconductor film 12 using photolithography and dry etching by the RIE method.

Thereafter, P- or N- type impurity ions 16 corresponding to the type of a transistor to be formed are doped into the p-Si film 12 except the region covered with the gate electrode 15 through the first and second gate insulating films 13 and 14, with the gate electrode 15 acting as a mask. This ion doping creates an intrinsic or substantially intrinsic region of the p-Si film 12 beneath the gate electrode 15.

Step 3 (Fig. 2C):

15 A resist 17 having a smaller width than the p-Si film 12 is formed so as to cover the gate electrode 15 and the second insulating film 14. Then, impurity ions 18 are doped into the p-Si film 12 to form LDD (Lightly Doped Drain) regions 12LD having a low density of doped ions, source 12s and drain 12d 20 having a high density of doped ions.

Thus, in the p-Si film 12, a region located right beneath the gate electrode 15 corresponds to a channel 12c, whereas regions located on both sides of the gate electrode 15 correspond to the source 12s and the drain 12d, respectively.

25 Step 4 (Fig. 2D):

Subsequent to removal of the resist 17, an SiN film 19 and an SiO<sub>2</sub> film 20 are sequentially stacked on the entire surface of the substrate 10 including the p-Si film 12 by the plasma CVD method, to form an interlayer insulating film comprising 5 two films, namely the SiN film 19 and the SiO<sub>2</sub> film 20.

After forming the SiN film 19 and the SiO<sub>2</sub> film 20, first contact holes 30 are formed through the interlayer insulating film at positions corresponding to the source 12s and the drain 12d, respectively, so as to reach the p-Si film 12. Then, a 10 source electrode 21 and a drain electrode 22 comprising aluminum or the like are formed in these first contact holes 30, respectively. Further, a planarization layer 23 comprising an organic resin or the like is deposited over these electrodes. Another contact hole 32 is then formed at a 15 position of the planarization layer 23 corresponding to the source electrode 21, into which an ITO, a transparent electrode material, is deposited and patterned to form a pixel electrode 24.

While the TFT employing a p-Si film is advantageous due to 20 its high mobility or the like as already described, the p-Si film has many crystalline defects at the grain boundaries and therefore electrons moving in the film tend to be easily trapped. It is particularly undesirable to have such crystalline defects in the channel region in a TFT. Therefore, 25 it has been proposed that hydrogen be introduced in the film so as to terminate dangling bonds existing in these defects. In

order to introduce hydrogen into the film, a method is known in which an SiN film containing a great number of hydrogen atoms is heated together with the p-Si film such that the hydrogen ions are transferred from the SiN film to the p-Si film. In 5 this case, it is preferable that the SiN film and the p-Si film be located as close to each other as possible so as to supply the hydrogen (H) atoms in the SiN film to the p-Si film by heating. However, if the p-Si film and the SiN film are directly in contact with each other, the threshold values of 10 the TFT employing such p-Si film vary due to predetermined charges generated in the SiN film. For this reason, in the above-mentioned top-gate type TFT, the SiN film 14 cannot be provided, as a gate insulating film, directly on the p-Si film 12, but the SiN film 14 must be formed on the SiO<sub>2</sub> film 13 15 disposed on the p-Si film 12, resulting in a structure employing two gate insulating films, as shown in Figs. 1, and 2A to 2D.

However, in a case where the gate insulating films comprise a sequence of two layers, namely the SiO<sub>2</sub> film 13 and 20 the SiN film 14 in the above-mentioned top-gate type TFT, the acceleration energy must be increased when doping ions into the semiconductor film so as to reach the p-Si film 12 through these two-layered gate insulating films. For example, phosphorus (P) ions must be doped with an acceleration energy 25 of 100keV or more. This may increase the power consumption of a doping apparatus.

Further, when the acceleration energy is increased for ion doping, the temperature of the substrate rises to as high as approximately 200 °C. Such a high temperature deteriorates the resist 17 covering the gate electrode 15 and the LDD regions, 5 which results in distortion in the periphery of the resist or makes the resist 17 difficult to peel off when removing it after ion doping.

#### SUMMARY OF THE INVENTION

10 The present invention is made in view of the foregoing problems of the related art, and aims to provide a method of manufacturing a thin film transistor capable of suppressing a temperature rise in a substrate at the time of ion doping with high acceleration energy.

15 In accordance with one aspect of the present invention, there is provided a method of manufacturing a thin film transistor comprising the steps of forming a semiconductor film on one major surface of a substrate; forming a first gate insulating film and a second gate insulating film sequentially 20 in this order on said semiconductor film; forming a gate electrode on said second gate insulating film; removing a part or all of said second gate insulating film except a region covered by said gate electrode; and, after removing said second gate insulating film, doping ions in said semiconductor film 25 with said gate electrode acting as a doping mask.

In another aspect of the present invention, there is provided a thin film transistor comprising a semiconductor film, a first gate insulating film, a second gate insulating film, and a gate electrode sequentially formed on one major surface of a substrate in that order, wherein said first gate insulating film covers said semiconductor film, and said second gate insulating film is formed by a material for supplying hydrogen to said semiconductor film only in a region covered by said gate electrode to have substantially the same shape as said gate electrode.

In another aspect of the present invention, there is provided a thin film transistor comprising a semiconductor film, a first gate insulating film, a second gate insulating film, and a gate electrode sequentially formed in that order on one major surface of a substrate, wherein said first gate insulating film covers said semiconductor film, and said second gate insulating film is formed by a material for supplying hydrogen to said semiconductor film and has a smaller film thickness in a region not covered with said gate electrode than that in a region covered by said gate electrode.

In still another aspect of the present invention, in said thin film transistor or said method of manufacturing the same, said first gate insulating film is a silicon oxide film and said second gate insulating film is a silicon nitride film.

In still another aspect of the present invention, said second gate insulating film is a supply source for supplying

hydrogen to said semiconductor film, and hydrogen contained in said second gate insulating film can be introduced into said semiconductor film by a predetermined annealing process.

In yet another aspect of the present invention, said 5 semiconductor film is a poly-silicon film.

In still another aspect of the present invention, after said gate electrode is formed in a predetermined pattern, said second gate insulating film is removed by etching with said gate electrode acting as a mask.

10 According to the TFT manufacturing method of the present invention, only the ion acceleration energy through the first gate insulating film or the second gate insulating film having a decreased thickness is required when ions are doped so as to form the source and the drain, thereby suppressing the 15 temperature of the substrate which rises in proportion to the acceleration energy.

#### BRIEF DESCRIPTION OF THE DRAWINGS

These and other objects of the invention will be explained 20 in the description below, in connection with the accompanying drawings, in which:

Fig. 1 is a cross section of a TFT manufactured by a TFT manufacturing method according to a related art;

Figs. 2A, 2B, 2C, and 2D are cross sections of a TFT for 25 explaining the manufacturing process steps of a related art;

Fig. 3 is a cross section of a TFT manufactured by a TFT manufacturing method according to the present invention; and

Figs. 4A, 4B, 4C, 4D and 4E are cross sections of a TFT for explaining the manufacturing process steps of the present invention.

#### DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

A preferred embodiment of the present invention, being a method of manufacturing a TFT according to the present invention, will be described in further detail with reference to the accompanying drawings. Fig. 3 is a cross section of a TFT manufactured in accordance with the present invention.

Referring to Fig. 3, a TFT manufactured in accordance with the present invention is differs from a TFT manufactured using the related art method described earlier in that the second gate insulating film 14 comprising an SiN film is etched using the gate electrode 15 as a mask such that this film 14 is not formed except on the region corresponding to the gate electrode 15.

The TFT manufacturing process steps of the present invention will be described with reference to the cross sections shown in Figs. 4A to 4E.

Step 1 (Fig. 4A):

On an insulating substrate 10 comprising a quartz glass, non-alkali glass, or the like, an SiO<sub>2</sub> film 11 serving as an insulating protective film is formed by the plasma CVD method,

and an a-Si film 12 is formed on the SiO<sub>2</sub> film 11 using a plasma CVD method. Then, the a-Si film 12 is subjected to annealing by scanning to irradiate the surface thereof with an excimer laser [XeCl] beam such that the a-Si film 12 is molten 5 and recrystallized to a p-Si film 12, which is then etched into an island shape functioning as an active layer of a p-Si TFT.

Step 2 (Fig. 4B):

A first gate insulating film 13 comprising an SiO<sub>2</sub> film and a second gate insulating film 14 comprising an SiN film are 10 formed over the entire surface of the p-Si film 12 by the CVD method. A conductive material comprising a refractory metal such as Cr or Mo is deposited on the second gate insulating film 14 by sputtering using photolithography and dry etching by the RIE method so as to form a gate electrode 15 such that it 15 superposes the semiconductor film 12. While the gate electrode 15 is formed, a gate signal line (not shown) connected to the gate electrode 15 for supplying gate signals is simultaneously formed.

Step 3 (Fig. 4C):

20 The second gate insulating film 14 is removed by etching with the gate electrode 15 acting as a mask such that the second gate insulating film 14 is left on the region beneath the gate electrode 15. Then, P- or N- type impurity ions 16 corresponding to the type of a transistor to be formed are 25 doped into the p-Si film 12 except the region covered with the gate electrode 15 and the second gate insulating film 14.

Thus, (the region of) the p-Si film 12 disposed beneath the gate electrode 15 becomes intrinsic or substantially intrinsic, into which no impurity ions are doped.

Step 4 (Fig. 4D):

5        A resist 17 having a smaller width than the p-Si film 12 is formed so as to cover the gate electrode 15 and the second insulating film 14. Then, impurity ions 18 are doped into the p-Si film 12 with the resist 17 acting as a mask, to form LDD (Lightly Doped Drain) regions 12LD having a low density of 10 doped ions, and source 12s and drain 12d having a high density of doped ions.

At this point, heating is applied to activate doped impurities and cause hydrogen atoms contained in the SiN film, that is the second gate insulating film 14, to be introduced 15 into the p-Si film 12 for hydrogenation.

As a result of the aforementioned process, in the p-Si film 12, the region located beneath the gate electrode 15 corresponds to a channel 12c, and the regions located on both sides of the gate electrode 15 correspond to the source 12s and 20 the drain 12d, respectively.

It should be noted that P-type ions such as boron (B) are doped for forming a P-channel type TFT whereas N-type ions such as phosphorus (P) are doped for forming an N-channel type TFT.

Step 5 (Fig. 4E):

25        Subsequent to removal of the resist 17, an SiN film 19 and an SiO<sub>2</sub> film 20 are sequentially stacked on the entire surface

of the substrate 10 including the p-Si film 12 by a plasma CVD method, to constitute an interlayer insulating film comprising two layers, namely the SiN film 19 and the SiO<sub>2</sub> film 20.

After forming the SiN film 19 and the SiO<sub>2</sub> film 20, first contact holes 30 are formed through the interlayer insulating film at positions corresponding to the source 12s and the drain 12d, respectively, so as to reach the p-Si film 12. Then, a source electrode 21 and a drain electrode 22 comprising aluminum or the like are formed in these first contact holes 30, respectively. Then, a planarization layer 23 comprising an organic resin or the like is deposited on these electrodes. Another contact hole 32 is then formed at a position of the planarization layer 23 corresponding to the source electrode 21, into which an ITO, a transparent electrode material, is deposited and patterned to form a pixel electrode 24. By the foregoing processes, a p-Si TFT semiconductor element is formed.

As described above, the first gate insulating film 13 comprising an SiO<sub>2</sub> film, which serves as a lower layer, and the second gate insulating film 14 comprising an SiN film, which serves as an upper layer, are stacked and thereafter the second gate insulating film 14 is removed by etching with the gate electrode 15 as a mask. Therefore, it is sufficient to dope ions through only the first gate insulating film 13, which allows ions to be sufficiently doped in the p-Si film 12 with only a low acceleration energy.

Also, when forming the LDD regions, ions can be doped with such an acceleration energy that does not cause deterioration of the resist covering the LDD regions

Thus, power consumption of the ion doping apparatus can be suppressed and also deterioration of the resist at the time of ion doping can be prevented.

In order to improve the TFT characteristics, hydrogen atoms contained in the SiN film are supplied to the p-Si film by heating, as described above. In this case, it is suffice to supply hydrogen atoms to at least the channel of the p-Si film, for the following reason. Namely, in the LLD regions (12LDs) as well as in the source and the drain (12s, 12d), the influence of dangling bonds in the p-Si film on the conductivity of the film is small because impurities are doped to these regions. To the contrary, the channel region of the p-Si film, which is intrinsic, will suffer great disadvantage in the operation characteristics of the TFT unless dangling bonds are terminated in this region of the film. According to the present invention, it is possible to effectively supply hydrogen atoms to the channel region due to the SiN film which is formed to be left only beneath the gate electrode.

Although the foregoing embodiment describes a case where an a-Si film is irradiated with a laser to obtain a p-Si film which functions as an active layer, a similar advantage can be achieved when a p-Si film is directly formed on an insulating protective film using a CVD method or the like.

The insulating protective film is provided so as to block sodium ions or the like from intruding into the p-Si film if a glass or the like is employed as a substrate 10. Therefore, the insulating protective film is not necessary when a 5 substrate causing no such impurity intrusion is employed. However, the insulating protective film is necessary when the substrate is not an insulating substrate.

Further, in the foregoing embodiment, the source electrode 21 is formed by filling the contact hole 30 provided 10 corresponding to the source 12s with Al, and the pixel electrode 24 comprising ITO is further formed so as to make contact with the source electrode 21. However, the present invention is not limited to that example, and it is also possible to fill the contact hole 30 with an ITO to form the 15 pixel electrode 24 directly in contact with the source 12s.

Although the foregoing embodiment describes an advantage of preventing deterioration of the resist for forming the LDD regions, the following advantage can be also achieved. Namely, in a TFT including an N-channel type TFT and a P-type channel 20 TFT on the same substrate, a resist is provided for one channel type TFT so as to prevent ions of the other channel type from being doped thereto when ions of the other type are doped. In such a case, it is possible to ensure that the resist will not be difficult to peel off after ion doping is completed.

25 Further, although the second gate insulating film 14 is removed such that the second gate insulating film 14 is etched

to have substantially the same shape as the gate electrode 15 in the foregoing example, the second gate insulating film 14 may be etched such that a desired thickness is left in certain regions of the second gate insulating film 14 other than the 5 region corresponding to the gate electrode 15, as shown by a dot line in Figs. 3, 4C, 4D, and 4E. In other words, in the second gate insulating film 14, the thickness of the regions excluding the region corresponding to the gate electrode 15 may be smaller than the thickness of the region corresponding to 10 the gate electrode 15. For example, when the thickness of the second gate insulating film 14 prior to etching is 400 Å, the thickness of the second gate insulating film 14 in the regions other than the region corresponding to the gate electrode 15 is reduced, by etching, to 100 to 200 Å (approximately 150 Å in 15 the average). This results in the second gate insulating film 14 having a thickness of 400 Å in the region corresponding to the gate electrode 15 and a thickness of 200 to 150 Å in the remaining region. Specifically, a certain thickness which does not block ion doping into the source and drain regions will 20 suffice. With an SiN film of such a thickness covering an entire semiconductor layer, sufficient ion doping can be achieved while preventing intrusion of impurities or the like, to thereby improve reliability of the TFT.

While the preferred embodiment of the present invention 25 has been described using specific terms, such description is for illustrative purposes only, and it is to be understood that

changes and variations may be made without departing from the spirit or scope of the appended claims.

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What is claimed is:

1. A method of manufacturing a thin film transistor comprising the steps of:

5 forming a semiconductor film on one major surface of a substrate;

forming a first gate insulating film and a second gate insulating film sequentially in this order on said semiconductor film;

10 forming a gate electrode on said second gate insulating film;

removing a part or all of said second gate insulating film except a region covered by said gate electrode; and

15 after removing said second gate insulating film, doping ions in said semiconductor film with said gate electrode acting as a doping mask.

2. The method according to claim 1, wherein said first gate insulating film is a silicon oxide film and said second gate insulating film is a silicon nitride film.

20 3. The method according to claim 1, wherein said second gate insulating film is a supply source for supplying hydrogen to said semiconductor film.

4. The method according to claim 3, wherein hydrogen contained in said second gate insulating film is introduced into said semiconductor film by a predetermined annealing process.

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5. The method according to claim 3, wherein said semiconductor film is a poly-silicon film.

6. The method according to claim 1, wherein after said gate electrode is formed in a predetermined pattern, said second gate insulating film is removed by etching with said gate electrode acting as a mask.

7. A thin film transistor comprising a semiconductor film, a first gate insulating film, a second gate insulating film and a gate electrode sequentially formed in that order on one major surface of a substrate,

wherein said first gate insulating film covers said semiconductor film, and

20 said second gate insulating film is made of a material for supplying hydrogen to said semiconductor film and is formed only in a region covered by said gate electrode to have substantially the same shape as said gate electrode.

8. The thin film transistor according to claim 7, wherein  
said first gate insulating film is a silicon oxide film and  
said second gate insulating film is a silicon nitride film.

5 9. The thin film transistor according to claim 7, wherein  
said semiconductor film is a poly-silicon film.

10. A thin film transistor comprising a semiconductor  
film, a first gate insulating film, a second gate insulating  
10 film and a gate electrode sequentially formed on one major  
surface of a substrate in that order,

wherein said first gate insulating film covers said  
semiconductor film, and

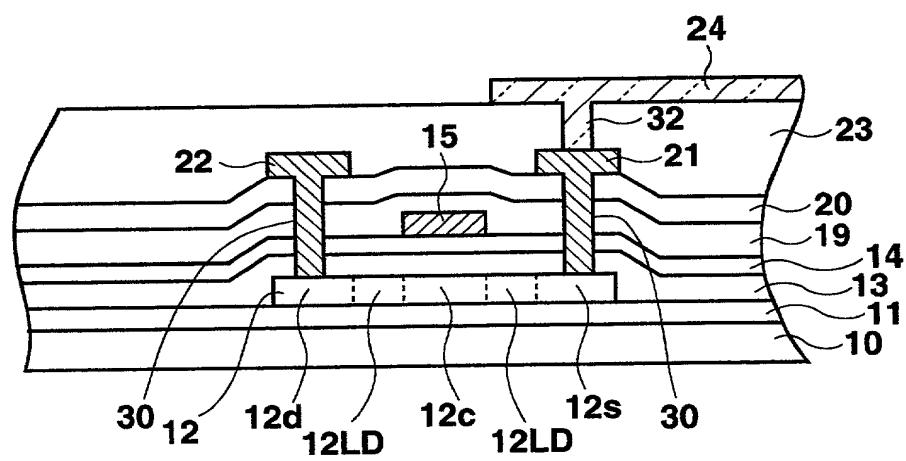
15 said second gate insulating film is made of a material for  
supplying hydrogen to said semiconductor film and has a smaller  
film thickness in a region not covered with said gate electrode  
than that in a region covered with said gate electrode.

20 11. The thin film transistor according to claim 10,  
wherein said first gate insulating film is a silicon oxide film  
and said second gate insulating film is a silicon nitride film.

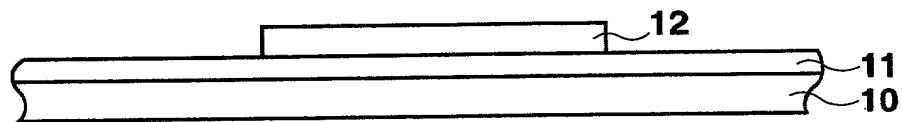
12. The thin film transistor according to claim 10,  
wherein said semiconductor film is a poly-silicon film.

ABSTRACT OF THE DISCLOSURE

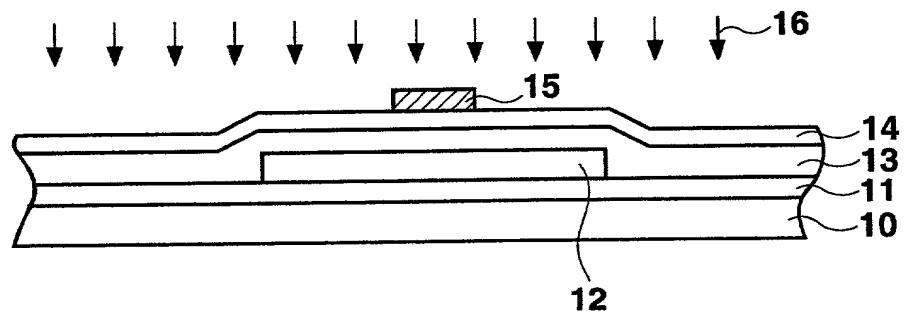
On a glass substrate (10), an insulating protective layer (11) comprising SiO<sub>2</sub> film is formed, and an active layer (12) comprising a p-Si film (12) is formed thereon. Further, a first gate insulating film (13) comprising an SiN film which serves as a lower layer and a second gate insulating film (14) comprising an SiN film which serves as an upper layer are stacked thereon. The second gate insulating layer (14) is then removed by etching with a gate electrode (15) formed thereon acting as a mask. Thus, ions can be doped only through the first gate insulating film (13) to the p-Si film (12) with a low acceleration energy.



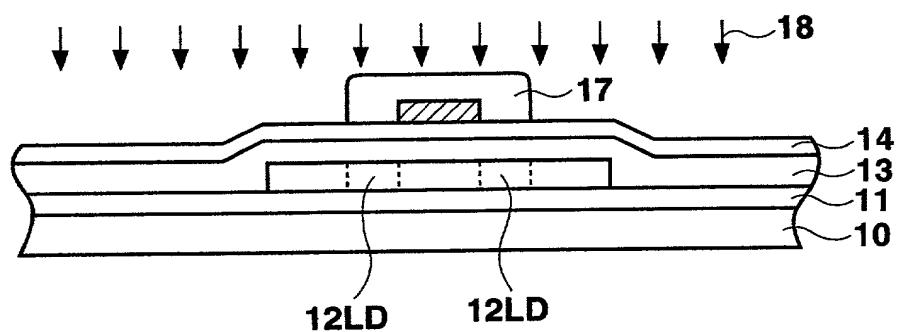
**Fig. 1 RELATED ART**



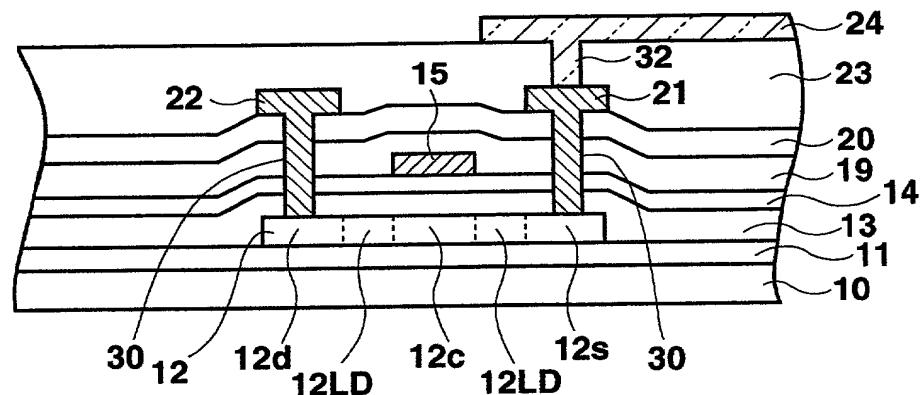
**Fig. 2A RELATED ART**



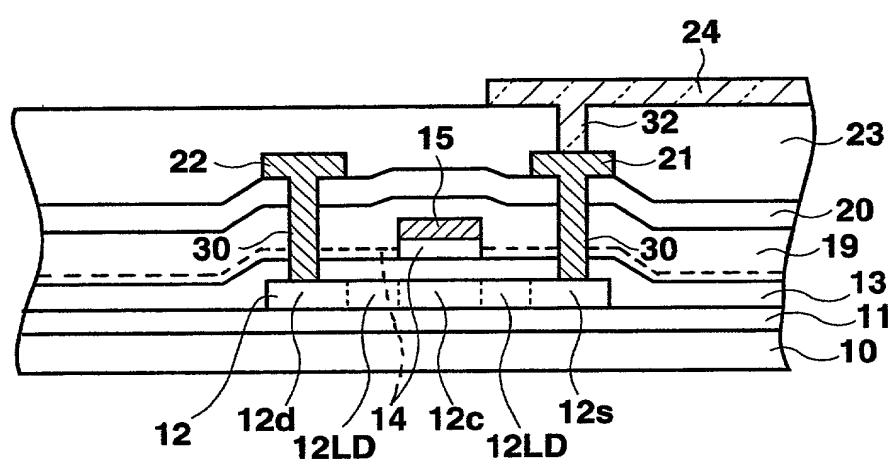
**Fig. 2B RELATED ART**



**Fig. 2C RELATED ART**

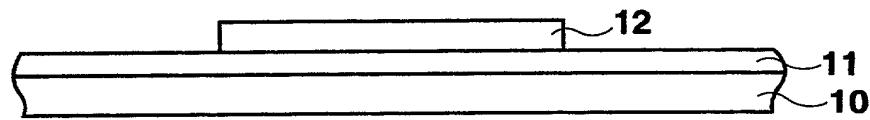


**Fig. 2D RELATED ART**

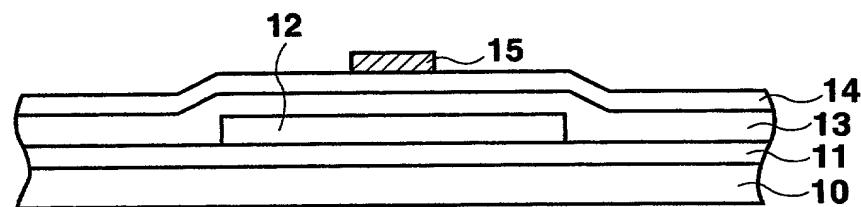


**Fig. 3**

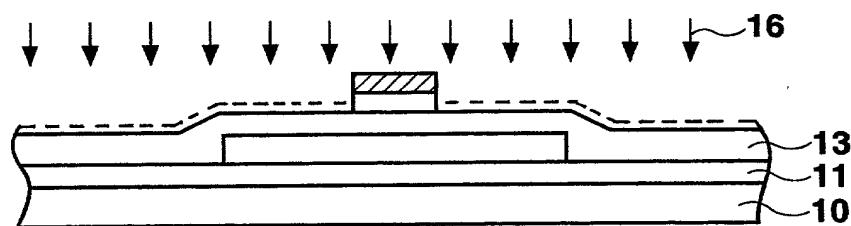
**Fig. 4A**



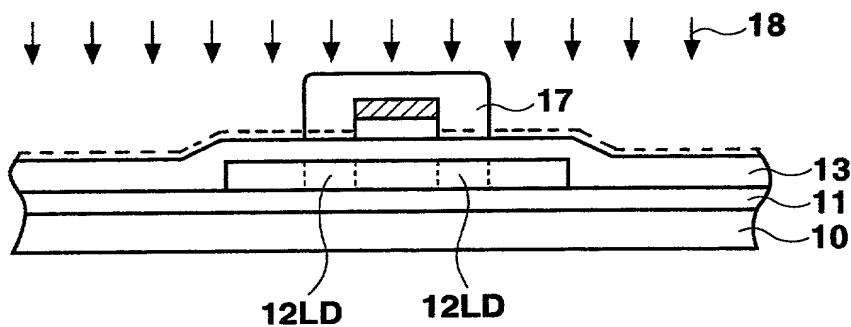
**Fig. 4B**



**Fig. 4C**



**Fig. 4D**



**Fig. 4E**

